



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,633	06/27/2003	Rajeev Joshi	018865-004210US	8725
20350	7590	09/15/2004	EXAMINER	
TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR SAN FRANCISCO, CA 94111-3834			BREWSTER, WILLIAM M	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 09/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/607,633

**Applicant(s)**

JOSHI ET AL.

**Examiner**

William M. Brewster

**Art Unit**

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 June 2004.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 7-25 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 7-25 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

Art Unit: 2823

## DETAILED ACTION

### *Generally*

The following rejection supercedes the rejection sent 5 August 2004.

### *Double Patenting*

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 7-17 provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 7-17 of copending Application No. 10/702,792.

This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7, 8, 14, 18, 20, 24 are rejected under 35 U.S.C. 102(b) as being anticipated by McShane et al., U.S. Patent No. 5,147,821.

McShane anticipates a method of making a chip device, the method comprising: in fig. 1, providing a leadframe 16 that includes leads 20; providing a die 12 that includes a metallized backside 14; coupling the die to the leadframe, limitations from claims 8, 14, further comprising configuring the plurality of leads 20; wherein the leadframe is mine is provided with preformed leads, leads having a preformed shape before attachment; col. 3, line 30 - col. 4, line 28; and encapsulating the die with a body 22 such that, in fig. 4, the metallized backside of the die is adjacent a window defined within the body 56, col. 7, line 35-51;

limitations from claim 17, using solder balls, not labeled, but shown at the end of leads 20, wherein coupling of the second of the two dies to the leadframe is performed, where the dies would be attached to different pads, and , col. 9, lines 6-32;

Art Unit: 2823

leadframe is performed, where the dies would be attached to different pads, and , col. 9, lines 6-32;

in fig. 4, wherein the backside of the semiconductor die, covered by metallization 54, is exposed 56 through the window of the molding compound and wherein the backside is substantially flush with the exterior surface of the molding compound, wherein the thickness of 52 is heuristic and may be quite thin in addition to “substantially flush” being subjective to the observer, col. 7, line 35 - col. 8, line 10;

limitations from claim 20, in fig. 5, the method further comprising mounting a second semiconductor die, represented by A and B, including a second backside to the leadframe, wherein second backside is exposed through a second window in the molding compound, 77 and 78, col. 8, lines 22-40; limitations from claim 24, wherein ends of the leads are co-planar with the backside of the semiconductor die, in fig. 1, wherein the distal ends of leads 20 attached to pieces 18 are co-planar with the backside of the semiconductor die 12.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over McShane as applied to claims 7, 8, 14, 18, 20, 24 above, and further in view of Maejima et al., U.S. Patent No. 5,347,709.

McShane does not specify removing the resin flashing, but Maejima does. Maejima teaches a method, in fig. 14, further comprising removing dambars from the leadframe, removing mold flashes and resins from the leads, and solder plating the leads, col. 7, lines 44-63. Maejima gives motivation in col. 7, lines 44-63. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Maejima's process with McShane's invention would have been beneficial because the invention removes the negative bonding effects of the bonding.

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over McShane as applied to claims 7, 8, 14, 18, 20, 24 above, and further in view of Orso et al., U.S. Patent No. 6,018,686.

McShane does not specify marking of the body on a surface opposite the window, but Orso does specify body marking. Orso teaches a method

Art Unit: 2823

comprising marking the body of the chip with a laser, and with ink, col. 1, lines 24-37. Orso gives motivation in col. 1, lines 24-37. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Orso's process with McShane's invention would have been beneficial because the invention gives indicia to dies which may be useful for sorting dies that pass inspection from those that do not pass.

Claims 13, 15, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over McShane as applied to claims 7, 8, 14, 18, 20, 24 above, and further in view of Layher et al., U.S. Patent No. 4,678,358.

McShane does not specify using preplated leads, but Layher does. Layher teaches in figs. 1 and 2 forms lead frame 10 provided with preplated leads 11, p. 4, lines 25-41, and col. 2, line 47 - col. 3, line 10. Layher gives motivation in col. 2, lines 6-21. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Layher's process with McShane's invention would have been beneficial because the invention does not subject the parts to a working temperature that will diffuse or melt the coating.

Claims 16,17, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over McShane as applied to claims 7, 8, 14, 18, 20, 24 above, and further in view of Fosberry et al., U.S. Patent No. 6,214,640.

Art Unit: 2823

McShane does not specify using posts for attaching dies, but Fosberry does. Fosberry teaches in fig. 11, wherein the die 12 is coupled to the leadframe 22 die attach pad and post, col. 10, lines 16-57, via solder bumps (not shown), and wherein the solder bumps are reflowed, col. 15, line 53 - col. 16, line 38. Fosberry gives motivation in col. 2, lines 21-55. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Fosberry's process with McShane's invention would have been beneficial because the invention allows encapsulation without prefabricated support structure.

Claims 19, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over McShane as applied to claims 7, 8, 14, 18, 20, 24 above, and further in view of Merrill, U.S. Patent No. 5,654,206.

McShane does not specify the common use of transistors in his chips, but Merrill does. Merrill in fig. 1 shows semiconductor die 10 with bonding pads 13 and 14, col. 2, lines 17-39, and in col. 1, lines 17-28 describes attaching the leads to power transistor and gate and source leads. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Merrill's process with McShane's invention would have been beneficial because the invention makes efficient connections between the transistors and the leads.



Art Unit: 2823

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*William M. Brewster*

4 August 2004  
WB